AMENDMENTS TO THE CLAIMS

Claims 1-45 (Cancelled)

46. (New) A MOS transistor formed in a semiconductor material of a first conductivity type, the MOS transistor comprising:

a plurality of source strips of a second conductivity type formed in the semiconductor material, each source strip having a depth, a length, and a width;

a plurality of drain strips of the second conductivity type formed in the semiconductor material such that a drain strip lies between each adjacent pair of source strips, each drain strip having the depth, the length, and a width;

a plurality of channel strips located between the source and drain strips such that a channel strip is located between each adjacent source and drain strip;

a plurality of gate strips formed over the channel strips between source strips and drain strips, the plurality of gate strips being isolated from the plurality of channel strips; and

a single source metal region formed over the plurality of source and drain strips to make electrical connections with the plurality of source strips, the single source metal region covering more than 25% and less than 50% of the plurality of source and drain strips.

47. (New) The MOS transistor of claim 46 and further comprising a single drain metal region formed over the plurality of source and drain strips to make electrical connections with the plurality of drain strips, the single drain metal region covering more than 25% and less than 50% of the plurality of source and drain strips.

48. (New) The MOS transistor of claim 46 wherein the width of a source strip is wider than the width of a drain strip.

49. (New) The MOS transistor of claim 46 wherein a gate strip has a serpentine shape.

50. (New) The MOS transistor of claim 46 wherein each gate strip is electrically connected together.

51. (New) The MOS transistor of claim 46 and further comprising:

a MOS device having a source connected to a ground node, a gate, and a drain electrically connected to the plurality of drain strips; and

a gate signal generator that outputs a first gate signal to the plurality of gate strips, a second gate signal to the gate of the MOS device, and a control signal, the first and second gate signals being non-overlapping;

a first switch connected to the control signal, and the semiconductor material of the first conductivity type;

a second switch connected to the ground node and the control signal; and

a resistor that is connected to the semiconductor material of the first conductivity type, a current flowing through the resistor to the ground node when the second switch is closed, and not flowing when the second switch is open.

52. (New) The MOS transistor of claim 51 wherein the control signal has a logic state opposite to the logic state of the first gate signal.

53. (New) The driver of claim 51 and further comprising:

a third switch connected to the second switch and the resistor that is controlled by an enable signal; and

a fourth switch connected to a voltage source and the resistor that is controlled by the enable signal.

54. (New) A MOS transistor formed in a semiconductor material of a first conductivity type, the MOS transistor comprising:

a plurality of source strips of a second conductivity type formed in the semiconductor material, each source strip having a depth, a length, and a width;

a plurality of drain strips of the second conductivity type formed in the semiconductor material such that a drain strip lies between each adjacent pair of source strips, each drain strip having the depth, the length, and a width, the width of a source strip being greater than a width of a drain strip;

a plurality of channel strips located between the source and drain strips such that a channel strip is located between each adjacent source and drain strip; and

a plurality of gate strips formed over the channel strips between source strips and drain strips, the plurality of gate strips being isolated from the plurality of channel strips.

55. (New) The MOS transistor of claim 54 and further comprising a single source metal region formed over the plurality of source and drain strips to make electrical connections with the plurality of source strips, the single source metal region covering more than 25% and less than 50% of the plurality of source and drain strips.

56. (New) The MOS transistor of claim 55 and further comprising a single drain metal region formed over the plurality of source and drain strips to make electrical connections with the plurality of drain strips, the single drain metal region covering more than 25% and less than 50% of the plurality of source and drain strips.

57. (New) The MOS transistor of claim 54 wherein a gate strip has a serpentine shape.

58. (New) The MOS transistor of claim 54 wherein each gate strip is electrically connected together.

59. (New) The MOS transistor of claim 54 and further comprising:

a MOS device having a source connected to a ground node, a gate, and a drain electrically connected to the plurality of drain strips; and

a gate signal generator that outputs a first gate signal to the plurality of gate strips, a second gate signal to the gate of the MOS device, and a control signal, the first and second gate signals being non-overlapping;

a first switch connected to the control signal, and the semiconductor material of the first conductivity type;

a second switch connected to the ground node and the control signal; and

a resistor that is connected to the semiconductor material of the first conductivity type, a current flowing through the resistor to the ground node when the second switch is closed, and not flowing when the second switch is open.

60. (New) The MOS transistor of claim 59 wherein the control signal has a logic state opposite to the logic state of the first gate signal.

61. (New) The driver of claim 59 and further comprising:

a third switch connected to the second switch and the resistor that is controlled by an enable signal; and

a fourth switch connected to a voltage source and the resistor that is controlled by the enable signal.